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1 The icewater language and interpreter 80%
Patrick A. D. Powell , Mohamed I. Elmasry
21st Proceedings of the Design Automation Conference on Design automation June 1984
A symbolic circuit design language for describing the topology and topography of a VLSI design in a simple and hierarchical manner is described. The language was intended to provide a simple manner of structuring a VLSI design, based on the Mead and Conway design methodology. Cells may be constructed from other cells and technology specific devices. Terminals for interconnecting cells are explicitly named, and may be accessed in a symbolic fashion from the language. The restriction of metho ...

2 Lessons from the design of the Eiffel libraries 77%
Bertrand Meyer
Communications of the ACM September 1990
Volume 33 Issue 9
The nature of programming is changing. Most of the software engineering literature still takes for granted a world of individual projects, where the sole aim is to produce specific software systems in response to particular requirements, little attention being paid to each system's relationship to previous or subsequent efforts. This implicit model seems unlikely to allow drastic improvements in software quality and productivity. Such order-of-magnitude advances will require a pr ...

3 Measuring designer performance to verify design automation systems 77%
D. E. Thomas , D. P. Siewiorek
Proceedings of the 14th design automation conference January 1977
This paper describes an experiment statistically designed to gather data on designers' performances in digital design situations. Results of the experiment not only provide data by which to calibrate the results of register transfer level computer aided design algorithms but also the variance to be expected among designers given identical tasks. The experimental techniques described here are applicable to other non-optimal algorithms such as wire routing.

4 Computer aided LSI circuit design: A relationship between topology and performance 77%
Paul Losleben
Proceedings of the 12th design automation conference January 1975
The relationship between topology and performance in LSI cell design requires a corresponding relationship between cell layout and circuit analysis computer programs. A computer aided design system demonstrating this is discussed.

5 Quantifying software designs 77%
John Beane , Nancy Giddings , Jon Silverman
Proceedings of the 7th international conference on Software engineering March 1984
This paper describes an effort to use metrics to evaluate software designs early in the design process. Key facets of the work include a machine processable design notation and the definition of software design metrics. We believe that the future success of building an intelligent software design assistant depends on the ability to quantify attributes of a software design, as well as to have the representation of the design available for automated examination.

6 Register allocation for free: The C machine stack cache 77%
David R. Ditzel , H. R. McLellan
Proceedings of the first international symposium on Architectural support for programming languages and operating systems March 1982
The Bell Labs C Machine project is investigating computer architectures to support the C programming language.1 One of the goals is to match an efficient architecture to the language and the compiler technology available. Measurements of different C programs show that roughly one out of every twenty instructions executed is either a procedure call or return.2 Procedure call overhead is therefore a very important consideration in the overall machine ...

7 An O(nlogm) algorithm for VLSI design rule checking 77%
C. R. Bonapace , C.-Y. Lo
Proceedings of the 1989 26th ACM/IEEE conference on Design automation conference June 1989
This paper describes a new variant of the segment tree approach for VLSI design rule checking. The best known algorithms to date for flat VLSI design rule checking require O(nlogn) expected time and O(√n) expected space, where n is the total number of edges on a mask layer of the chip. We present a new algorithm that can run in O(nlogm) expected time, where m is the m ...

8 Design for manufacturability and yield 77%
A. J. Strojwas
Proceedings of the 1989 26th ACM/IEEE conference on Design automation conference June 1989
This tutorial focuses on the design strategies for VLSI circuits that are aimed at achieving manufacturable, high-yielding chips. We review the current status of statistical design methodologies based upon statistically-valid modeling and process characterization approaches. Both parametric and functional yield maximization strategies are covered. This tutorial argues that by providing a better starting point for manufacturing, the profitability and competitiveness can be significantly impr ...

9 A structural view of the Cedar programming environment 77%
Daniel C. Swinehart , Polle T. Zellweger , Richard J. Beach , Robert B. Hagmann
ACM Transactions on Programming Languages and Systems (TOPLAS) August 1986
Volume 8 Issue 4
This paper presents an overview of the Cedar programming environment, focusing on its overall structure—that is, the major components of Cedar and the way they are organized. Cedar supports the development of programs written in a single programming language, also called Cedar. Its primary purpose is to increase the productivity of programmers whose activities include experimental programming and the development of prototype software systems for a high-performance personal computer. T ...

10 CHESHIRE: an object-oriented integration of VLSI CAD tools 77%
L.-P. Demers , P. Jacques , S. Fauvel , E. Cerny
24th ACM/IEEE conference proceedings on Design automation conference October 1987
We present an approach to the integration of VLSI CAD tools through the uniformization of interactions with design cells at both the user and the program levels. The integration model is based on the concept of objects applied to circuit cells. User interactions are achieved through a desk-top-like graphics interface. Regrouping of related or equivalent cell-objects into tissues represented by a generic cell helps with their management. Late binding of specific version cells then encourages ...

11 Layla: a VLSI layout language 77%
Warren E. Cory
Proceedings of the 22nd ACM/IEEE conference on Design automation June 1985
This paper describes Layla, a Pascal-based hardware description language for the specification of VLSI layouts. The primary application of Layla is the development of parameterized cell libraries. Important features include Pascal's computational power and file I/O facilities, hierarchical (cell-based) layout generation, a run-time design parameter file, an extendible layer set, external compilation, the ability to support different output formats, and the automatic generation of parameteri ...

12 Model order-reduction of RC(L) interconnect including variational analysis 77%
Ying Liu , Lawrence T. Pileggi , Andrzej J. Strojwas
Proceedings of the 36th ACM/IEEE conference on Design automation conference June 1999

13 Adaptive resource management for flow-based IP/ATM hybrid switching systems 77%
Hao Che , San-qi Li , Arthur Lin
IEEE/ACM Transactions on Networking (TON) October 1998
Volume 6 Issue 5

14 Guidance for the use of the Ada programming language in high integrity systems 77%
B. A. Wichmann
ACM SIGAda Ada Letters July 1998
Volume XVIII Issue 4
This paper is the current result of a study by the ISO HRG Rapporteur group which is being circulated for comment. Many people have contributed to this, but those who have either attended two recent meetings of group or have made substantial e-mail comments are: Praful V Bhansali (Boeing, USA), Alan Burns (University of York, UK), Bernard Carre' (Praxis Critical Systems, UK), Dan Craigen (ORA, Canada), Nick Johnson MoD, UK), Stephen Michell (Canada), Gilles Motet (DGEI/INSA, France), George Roma ...

15 Computer-generated floral ornament 77%
Michael T. Wong , Douglas E. Zongker , David H. Salesin
Proceedings of the 25th annual conference on Computer graphics and interactive techniques July 1998

16 Physical design challenges for performance 77%
David P. LaPotin , Uttam Ghoshal , Eli Chiprout , Sani R. Nassif
Proceedings of the 1997 international symposium on Physical design April 1997

17 Issues and experience in designing two-handed interaction 77%
Stephané Chatty
Conference companion on Human factors in computing systems April 1994

18 The use of description logics in KBSE systems: experience report 77%
Premkumar T. Devanbu , Mark A. Jones
Proceedings of the 16th international conference on Software engineering May 1994

19 SPARK—an annotated Ada subset for safety-critical programming 77%
Bernard Carré , Jonathan Garnsworthy
Proceedings of the conference on TRI-ADA '90 December 1990

20 Manufacturability of low power CMOS technology solutions 77%
A. J. Strojwas , M. Quarantelli , J. Borel , C. Guardiani , G. Nicollini , G. Crisenza , B. Franzini , J. Wiart
Proceedings of the 1996 international symposium on Low power electronics and design August 1996

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21 The use of description logics in KBSE systems 77%
Premkumar Devanbu , Mark A. Jones
ACM Transactions on Software Engineering and Methodology (TOSEM) April 1997
Volume 6 Issue 2
The increasing size and complexity of many software systems demand a greater emphasis on capturing and maintaining knowledge at many different levels within the software development process. This knowledge includes descriptions of the hardware and software components and their behavior, external and internal design specifications, and support for system testing. The Knowledge-based software engineering (KBSE) research paradigm is concerned with systems that use formally represented knowledg ...

22 Fortran 90: an entry to object-oriented programming for the solution of partial differential equations 77%
L. Machiels , M. O. Deville
ACM Transactions on Mathematical Software (TOMS) March 1997
Volume 23 Issue 1

23 The EM-X parallel computer: architecture and basic performance 77%
Yuetsu Kodama , Hirohumi Sakane , Mitsuhisa Sato , Hayato Yamana , Shuichi Sakai , Yoshinori Yamaguchi
ACM SIGARCH Computer Architecture News , Proceedings of the 22nd annual international symposium on Computer architecture May 1995
Volume 23 Issue 2
Latency tolerance is essential in achieving high performance on parallel computers for remote function calls and fine-grained remote memory accesses. EM-X supports interprocessor communication on an execution pipeline with small and simple packets. It can create a packet in one cycle, and receive a packet from the network in the on-chip buffer without interruption. EM-X invokes threads on packet arrival, minimizing the overhead of thread switching. It can tolerate communication latency by using ...

24 Creating reference architectures: an example from avionics 77%
Don Batory , Lou Coglianese , Mark Goodwin , Steve Shafer
ACM SIGSOFT Software Engineering Notes , Proceedings of the 1995 Symposium on Software reusability August 1995
Volume 20 Issue SI
ADAGE is a project to define and build a domain-specific software architecture (DSSA) environment for assisting the development of avionics software. A central concept of DSSA is the use of software system generators to implement component-based models of software synthesis in the target domain [SEI90].In this paper, we present the ADAGE component-based model (or reference architecture) for avionics software synthesis. We explain the modeling procedures used, review our initial g ...

25 Designing and implementing Choices: an object-oriented system in C++ 77%
Roy H. Campbell , Nayeem Islam , David Raila , Peter Madany
Communications of the ACM September 1993
Volume 36 Issue 9

26 VHDL 1076-1992 languages changes 77%

Andrew Guyler
Proceedings of the conference on European Design Automation November 1992

27 Metric-driven reengineering for static concurrency analysis 77%
David L. Levine , Richard N. Taylor
ACM SIGSOFT Software Engineering Notes , Proceedings of the 1993 international symposium on Software testing and analysis July 1993
Volume 18 Issue 3
An approach to statically analyzing a concurrent program not suited for analysis is described. The program is reengineered to reduce the complexity of concurrency-related activities, thereby reducing the size of the concurrency state space. The key to the reengineering process is a metric set that characterizes program task interaction complexity and provides guidance for restructuring. An initial version of a metric set is proposed and applied to two examples to demonstrate the utility of ...

28 Programming for events 77%
David S. Eastwood
ACM SIGAPL APL Quote Quad , Proceedings of the international conference on APL '91 July 1991
Volume 21 Issue 4
Modern windowing user interfaces offer both a challenge and an opportunity to the APL programmer. This paper discusses some of the factors that need to be taken into account when designing APL applications in a windowing environment. In such an environment the application programmer needs to design the application to react to events which occur in the environment rather than design the application to take over the environment, especially when a number of independent applications are being run si ...

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1 **Language support for multidisciplinary applications**
Mehrotra, P.; Van Rosendale, J.; Zima, H.P.;
IEEE Computational Science and Engineering [see also Computing in Science & Engineering] , Volume: 5 Issue: 2 , Apr-Jun 1998
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2 **Approaches for integrating task and data parallelism**
Bal, H.E.; Haines, M.;
Concurrency, IEEE [see also IEEE Parallel & Distributed Technology] , Volume: 6 Issue: 3 , Jul-Sep 1998
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3 **Quench simulation for 16T dipole built at Texas A&M University**
Latypov, D.; McIntyre, P.; Weijun Shen;
Particle Accelerator Conference, 1997. Proceedings of the 1997 , Volume: 3 , 12-16 May 1997
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4 **Teaching the design of a chip under the Cadence Opus environment using the Alliance cell libraries**
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Microelectronic Systems Education, 1997. MSE '97. Proceedings., 1997 IEEE International Conference on , 21-23 Jul 1997
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[Abstract] [PDF Full-Text (164 KB)] **IEEE CNF**

5 **VLSI design and realisation of a 4 input high speed fuzzy processor**
Gabrielli, A.; Gandolfi, E.; Masetti, M.; Roch, M.R.;
Fuzzy Systems, 1997., Proceedings of the Sixth IEEE International Conference on , Volume: 2 , 1-5 Jul 1997
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[Abstract] [PDF Full-Text (692 KB)] **IEEE CNF**

6 **Design and realization of a two input fuzzy chip running at a rate of 80 ns**
Falchieri, D.; Gabrielli, A.; Gandolfi, E.; Masetti, M.;
Fuzzy Information Processing Society, 1997. NAFIPS '97. 1997 Annual Meeting of the North American , 21-24 Sep 1997
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[Abstract] [PDF Full-Text (616 KB)] **IEEE CNF**

7 **Fast dynamic process migration**
Roush, E.T.; Campbell, R.H.;
Distributed Computing Systems, 1996., Proceedings of the 16th International Conference on , 27-30 May 1996
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[Abstract] [PDF Full-Text (732 KB)] **IEEE CNF**

8 **High level CAD melds microsystems with foundries**
Karam, J.M.; Courtois, B.; Bauge, M.;
European Design and Test Conference, 1996. ED&TC 96. Proceedings , 11-14 Mar 1996
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[Abstract] [PDF Full-Text (484 KB)] **IEEE CNF**

9 **An efficient method for the self-consistent electro-thermal simulation and its integration into a CAD framework**
Szekely, V.; Poppe, A.; Rencz, M.; Farkas, G.; Csendes, A.; Pahi, A.;
European Design and Test Conference, 1996. ED&TC 96. Proceedings , 11-14 Mar 1996
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[Abstract] [PDF Full-Text (168 KB)] **IEEE CNF**

10 **Runtime support for data parallel tasks**
Haines, M.; Hess, B.; Mehrotra, P.; Van Rosendale, J.; Zima, H.;
Frontiers of Massively Parallel Computation, 1995. Proceedings. 'Frontiers '95'., Fifth Symposium on the , 6-9 Feb 1995
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[Abstract] [PDF Full-Text (576 KB)] **IEEE CNF**

11 **A VLSI chip for template matching**
Ranganathan, N.; Venugopal, S.;
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12 **An efficient FSE/DFE-based HDSL equalizer with new adaptive algorithms**
Cheng-I Hwang; Tzu-Chiang Tang; Lin, D.W.; Sau-Gee Chen;
Communications, 1994. ICC 94, SUPERCOMM/ICC '94, Conference Record, Serving Humanity Through

Communications. IEEE International Conference on , 1-5 May 1994
Page(s): 288 -292 vol.1

[Abstract] [PDF Full-Text (368 KB)] **IEEE CNF**

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13 **An open system knowledge framework and its bridge evaluation application**
Wong, S.T.C.;
Systems, Man and Cybernetics, IEEE Transactions on , Volume: 24 Issue: 6 , Jun 1994
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14 **Two-dimensional Modeling Of Self-aligned Silicide Process With A General-purpose Process Simulater OPUS**
Kai, K.; Kuroda, S.; Nishi, K.;
VLSI Process and Device Modeling, 1993. (1993 VPAD) 1993 International Workshop on , 14-15 May 1993
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15 **Function-based recognition from incomplete knowledge of shape**
Stark, L.; Hoover, A.; Goldgof, D.; Bowyer, K.;
Qualitative Vision, 1993., Proceedings of IEEE Workshop on , 14 Jun 1993
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16 **A fault oriented partial scan design approach**
Chickermane, V.; Patel, J.H.;
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17 **Put a SPARC into your PC**
Lacey, T.;
Compcon Spring '91. Digest of Papers , 25 Feb-1 Mar 1991
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18 **Robust decentralized control laws for the ACES structure**
Collins, E.G., Jr.; Phillips, D.J.; Hyland, D.C.;
IEEE Control Systems Magazine , Volume: 11 Issue: 3 , Apr 1991
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[Abstract] [PDF Full-Text (672 KB)] **IEEE JNL**

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19 **SKILL: a CAD system extension language**
Barnes, T.J.;

Design Automation Conference, 1990. Proceedings. 27th ACM/IEEE , 24-28 Jun 1990
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20 **A fast three-dimensional process simulator OPUS/3D with access to two-dimensional simulation results**
Ushio, S.; Nishi, K.; Kuroda, S.; Kai, K.; Ueda, J.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 9 Issue: 7 , Jul 1990
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21 **A general-purpose two-dimensional process simulator-OPUS for arbitrary structures**
Nishi, K.; Sakamoto, K.; Kuroda, S.; Ueda, J.; Miyoshi, T.; Ushio, S.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , Volume: 8 Issue: 1 , Jan 1989
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